A 1–17-GHz InGaP–GaAs HBT MMIC Analog Multiplier and Mixer With Broad-Band Input-Matching Networks

Bosen Tzeng, Chun-Hsien Lien, Huei Wang, *Senior Member, IEEE*, Yu-Chi Wang, Pane-Chane Chao, *Senior Member, IEEE*, and Chung-Hsu Chen

***Abstract*—An InGaP–GaAs heterojunction bipolar transistor (HBT) analog multiplier/mixer monolithic microwave integrated circuit (MMIC) is developed that adopts a Gilbert-cell multiplier with broad-band input-matching networks to widen the bandwidth up to 17 GHz. This MMIC was fabricated using a commercially available 6-in InGaP–GaAs HBT MMIC process. It achieved a measured sensitivity of above 1100 V/W for an analog multiplier and a conversion gain of better than 9 dB for a mixer. It also demonstrated a lower corner frequency and noise than that of an InP HBT analog multiplier. The measured low-frequency noise was 10 nV/sqrt(Hz), which is about half of that of an InP HBT analog multiplier with a similar architecture. The corner frequency of the low-frequency noise was roughly estimated to be 15 kHz. The measured performance of this MMIC chip with gain–bandwidth–product (GBP) of 47 GHz rivals that of the reported GaAs-based analog multipliers and mixers. The high GBP result achieved by this chip is attributed to the HBT device performance and the broad-band input-matching network.**

***Index Terms*—Active mixer, analog multiplier, GaAs monolithic microwave integrated circuit (MMIC), Gilbert cell.**

I. Introduction

THE multiplication or mixing circuit is an important building block in signal-processing and communication systems. The mixer is a critical building block because it affects the overall system performance and the performance requirement of adjacent building blocks including low-noise amplifier (LNA), local oscillator (LO), RF filter, image-rejection filter, and IF stages [1]. The millimeter-wave multiplier is used for the modulation of high-speed data transmitted at microwave or millimeter-wave carrier frequencies [2].

The Gilbert-based multipliers and mixers have been demonstrated with various monolithic microwave integrated circuit (MMIC) technologies. High conversion gain of Gilbert-based mixers have been achieved by Si CMOS and Si bipolar junction transistor (BJT) technologies, but they fall short of providing bandwidth above 10 GHz [8], [9]. Record mixer RF bandwidth has been demonstrated using 0.1-μm InP high electron-mobility transistor (HEMT) technology with low gain [11]. With high f_T (70 GHz), the InP HBT-based analog mixer has demonstrated a record gain–bandwidth–product (GBP) of 116.4 GHz [2].

In this study, we have demonstrated a wide-bandwidth 1–17-GHz MMIC InGaP–GaAs HBT analog multiplier and mixer. The GaAs HBT active mixer is based on the Gilbert transconductance multiplier cell. Although the f_T of the device used in the design is only 40 GHz, significantly lower than that of the InP HBT device, our broad-band input-matching design resulted in wide bandwidth for this chip. The MMIC chip without RF, LO, and IF amplifiers also shows low-noise and high frequency-conversion performance compared with those of InP HBT analog multipliers and mixers. Table I summarizes published wide-band analog balanced mixer integrated-circuit (IC) gain-bandwidth performance. Our MMIC achieves a measured gain of 9.3 dB and bandwidth of 16 GHz and, thus, even without a pre- or post-amplifier, gives the highest GBP of 47 GHz among the reported GaAs-based analog active mixer.

TABLE I
SUMMARY OF PREVIOUSLY PUBLISHED WIDE-BAND ANALOG BALANCED MIXER IC GBP PERFORMANCE DEMONSTRATED WITH VARIOUS MMIC TECHNOLOGIES. $\mathrm{GBP} = 10(\mathrm{Gain(dB)}/20) \cdot \mathrm{Bandwidth(GHz)}$

	Device	Design Topology	Gain	Bandwidth	GBP
Kobayashi *et al.* [2]	InP HBT f_T=70 GHz	Gilbert cell with LO, RF and IF amplifier	15 dB	DC to 20 GHz	116.4 GHz
Burns *et al.* [6]	InP HBT f_T=90 GHz	Gilbert cell with LO drive and IF buffer	-6 dB	DC to 15 GHz	8 GHz
Kobayashi *et al.* [7]	InP HBT f_T=65 GHz	Gilbert cell with RF output buffer	2 dB	5 to 12 GHz	9 GHz
Umeda *et al.* [4]	GaAs HBT f_T=30 GHz	Gilbert cell with RF Darlington-coupled amplifier	22 dB	2.2 to 5.6 GHz	43 GHz
Osafune *et al.* [5]	GaAs HBT f_T=90 GHz	Gilbert cell	5 dB	DC to 20 GHz	36 GHz
Glenn *et al.* [10]	SiGe HBT f_T=47 GHz	Gilbert cell with IF buffer	5.5 dB	DC to 12 GHz	22 GHz
Wholey *et al.* [3]	Si BJT f_T=10 GHz	Gilbert cell	16 dB	DC to 6 GHz	38 GHz
Weger *et al.* [9]	Si BJT f_T=20 GHz	Gilbert cell	15 dB	DC to 8 GHz	45 GHz
This Work	GaAs HBT f_T=40 GHz	Gilbert cell with broadband input matching network	9.3 dB	1 to 17 GHz	47 GHz

Manuscript received July 30, 2001. This work was supported in part by the Research Excellence Program funded by the Ministry of Education, R.O.C., under Grant ME 89-N-FA01-1-1 and Grant ME 89-E-FA06-2-4, and by the National Science Council, R.O.C., under Grant NSC 89-2219-E-002-042 and Grant NSC 89-2213-E-002-178.

B. Tzeng was with the Graduate Institute of Communication Engineering, National Taiwan University, Taipei, 10617 Taiwan, R.O.C. He is now with MedTek Inc., Hsin-Chu City, 300 Taiwan, R.O.C.

C.-H. Lien and H. Wang are with the Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, 10617 Taiwan, R.O.C.

Y.-C. Wang, P.-C. Chao, and C.-H. Chen are with the WIN Semiconductors Corporation, Tao Yuan County, 333 Taiwan, R.O.C.

Digital Object Identifier 10.1109/TMTT.2002.804506

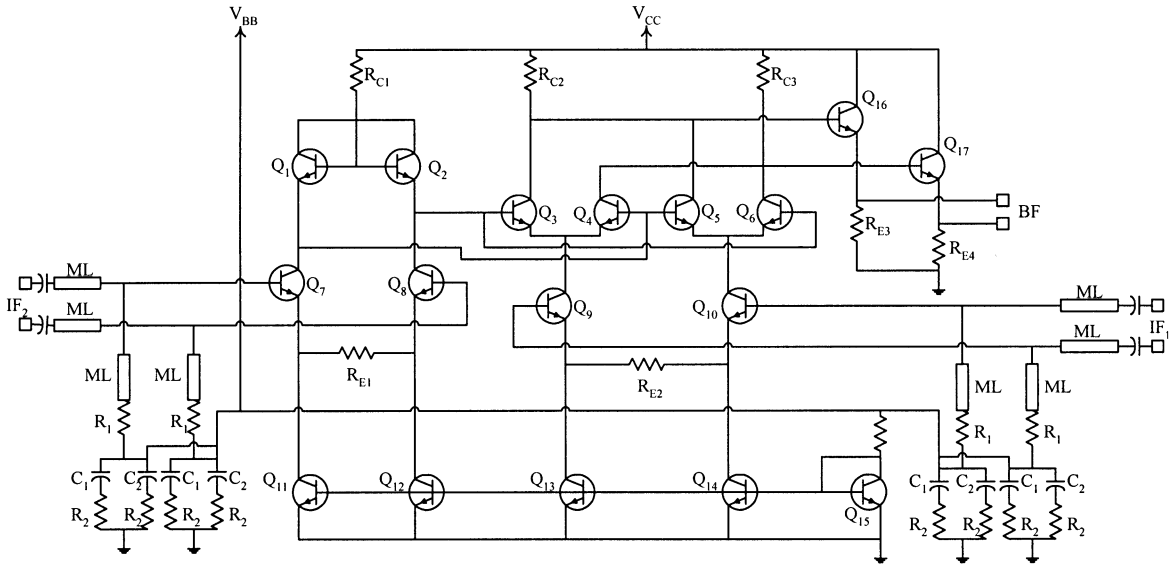


Fig. 1. Circuit schematic diagram of the 1–17-GHz analog multiplier and mixer.

II. Device Characteristics and MMIC Process

The MMIC reported in this paper is based on the 6-in InGaP–GaAs HBT device technology with an emitter finger width of 2 μm. The epitaxial layer structure features a metal–organic chemical vapor deposition (MOCVD) grown C-doped base, InGaAs emitter contact layer, mesa etch stops, and base ledge layer. Two metal layers are provided for interconnection. 50-$\Omega/\square$ TaN is used for thin-film resistors. Metal–insulator–metal (MIM) capacitors are realized with PECVD Si_3N_4 with a unit capacitance of 300 pF/mm^2. The backside process features a 100-μm-thick substrate, 50-μm-diameter standard through via holes, gold plating, and street etch.

The measured HBT dc-current gain is approximately 80 at a current density of $J_c = 9.5$ kA/cm^2. The common-emitter breakdown voltage $\mathrm{BV_{CEO}}$ is 15 V. The 2×20 μm^2 single-emitter HBTs used in the design achieve an f_T of 40 GHz and an $f_{\max}$ of 140 GHz at collector–emitter voltage ($\mathrm{V_{CE}}$) of 3 V.

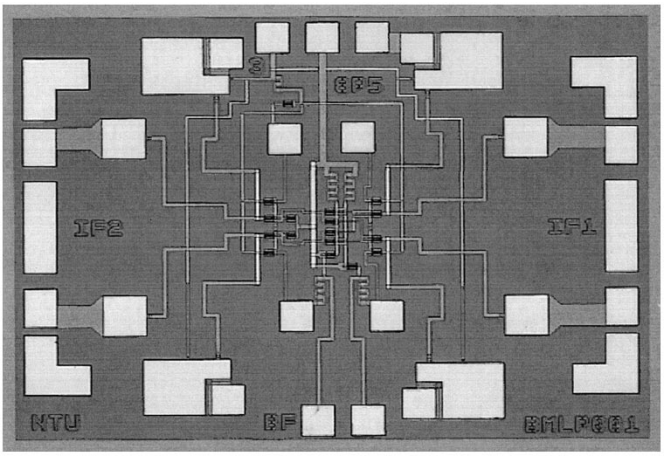


Fig. 2. 1-17-GHz analog multiplier and mixer chip photograph. The chip size is 2 mm × 1.5 mm. The mixer characteristics of the chip were measured using on-wafer probing on the IF1 as the RF input port and IF2 as the LO. While measuring the multiplier characteristics, the input signals were fed from the IF pads and the output was extracted from the BF pad.

III. Design of Analog Multiplier and Mixer

The schematic and microphotograph of the 1–17-GHz analog multiplier and mixer MMIC are shown in Figs. 1 and 2, respectively. Throughout the design, 2×20 μm^2 single-emitter HBTs are used to achieve high-frequency operation up to 20 GHz. The circuit (called BMLP001) can be divided into the: 1) predistortion circuit; 2) Gilbert cell core; 3) output buffer; 4) dc-bias circuit; and 5) input-matching network. The Gilbert cell core of the chip is series connected to an emitter couple pair (ECP) with two cross-coupled ECPs, at which frequency mixing takes place. The chip employs 50-Ω degenerating resistors for tradeoff between dynamic range and conversion gain. The output of the Gilbert cell core is directly fed into the output buffer, which consists of two emitter followers and performs the output match to 50 Ω. Current mirrors act as stable current sources. The dc-supply current is 3.7 mA, and the dc-supply voltages are 5.6 and 2.4 V, respectively. Total dc power consumption is 148 mW. The base voltages of the Gilbert cell are supplied through the input-matching short stubs and bypass capacitances, which prevent currents through the input-matching resistors. Two small resistors in series with the bypassing capacitances are included to damp out potential resonance. In order to achieve broad-band operation, the input network is used to match the capacitive-looking impedance of the ECPs at the upper band edge. The input-matching network is a series microstrip line with a shunt microstrip line terminated with a 50-Ω resistor. As shown in Fig. 3, without the matching circuitry, the conversion gain will slope down from 9 to 3 dB when the RF and LO frequency sweep from 1 to 17 GHz. Fig. 4 also shows the return losses of the two input ports are greatly improved to below 15 dB from 2 to 16 GHz with the broad-band input-matching circuitries.

The design procedures of this analog multiplier and mixer are summarized as follows. The emitter degenerating resistors

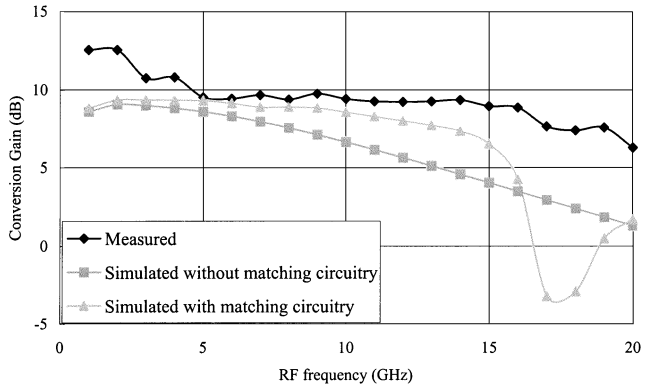


Fig. 3. Simulated and measured conversion gain of the chip. The chip has a measured conversion gain of 9.3 dB with a bandwidth of 1–17 GHz.

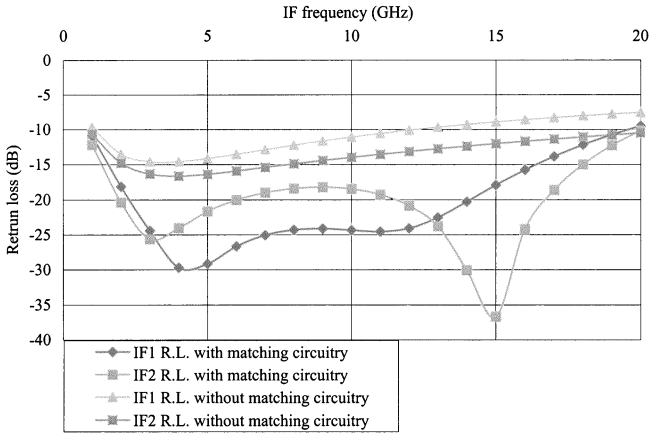


Fig. 4. Simulated input return loss of BMLP001 with and without input-matching circuitry. The return losses of the two input ports are greatly improved to below 15 dB from 2 to 16 GHz with the broad-band input-matching circuitries.

R_{E1} and R_{E2} should be chosen first, which would mainly determine the conversion gain of the circuit. After that, the input thin microstrip line is used to resonate out $C_{\rm be}$ at high frequency. This will make the second dip in the return loss. Finally, the output buffer collector current is determined according to $R_{\rm OUT} = 2 \cdot (V_T/I_C + R_C/\beta)$.

IV. Circuit Simulation and Measured Results

A. Circuit Simulation

The circuit shown in Fig. 1 was simulated using a harmonic-balance technique implemented in HP EESOF LIBRA [14] with the large-signal Gummel–Poon model. The model can effectively describe low-current drop in current gain, basewidth modulation, high-level injection, current-dependent base resistance, distributed base–collector capacitance, distributed phenomena in the base region, etc. Except for the circuit simulation using the harmonic-balance method, the input-matching circuits were simulated with a commercially available Sonnet Software Inc., Liverpool, NY, full-wave analysis tool [15] to insure the accuracy of passive models. The microstrip lines of the other portion of the layout were made as short as possible to reduce the distributed effect. The simulated results are discussed together with the measured results below.

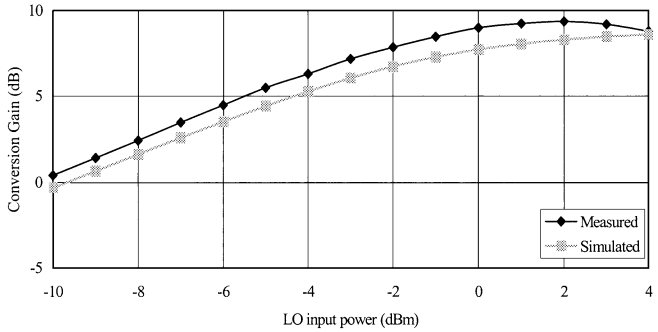


Fig. 5. Simulated and measured conversion gain versus LO input power. The measured LO saturation power is 2 dBm and the saturation conversion gain is 9.3 dB.

B. Measured Results

1) Mixer Characteristics: As labeled on the MMIC chip, the mixer characteristics of the chip were measured using on-wafer probing on IF1 as the RF input port and IF2 as the LO. The ground–signal–ground (GSG) probe was used at the RF input port. The other GSG pad was left open. It was measured using wire bonding of output pads as the IF output port. The output was then connected to a spectrum analyzer through dc-blocking capacitors. The conversion gain was measured at −20-dBm RF power. Fig. 5 shows the conversion gain as a function of LO power with RF frequency of 11 GHz and IF frequency of 10 MHz. Both simulation and measurement shows that the conversion gain almost saturated approximately 2 dBm of LO power. The conversion gain versus the RF frequency is shown in Fig. 3 with both RF and LO ports swept in frequency from 1 to 20 GHz, a fixed IF frequency of 10 MHz, and LO power of 2 dBm. The conversion gain is approximately 9.3 dB with a bandwidth of 1–17 GHz. The measured LO-to-RF isolation is approximately −80 dB at 1 GHz and goes up to −40 dB at 17 GHz with 0-dBm LO input drive.

2) Multiplier Characteristics: The multiplier characteristics of BMLP001 were measured with the same setup as the mixer measurement. Fig. 6 shows the output voltage as a function of input IF powers with IF frequency of 11 GHz and output baseband frequency (BF) of 10 MHz. Both simulation and measurement show the output voltage was linear below −11 dBm of IF power. The output voltage versus the IF frequency is shown in Fig. 7, with two IF ports swept in frequency from 1 to 20 GHz, a fixed IF frequency of 10 MHz, and IF power of −11 dBm. The sensitivity was approximately 1100 V/W with a bandwidth of 1–17 GHz. The measurements of output voltage versus input IF frequency were repeated on four MMIC chips of the same wafer, demonstrating consistent measured results, as shown in Fig. 7.

3) Low-Frequency Noise: To measure the low-frequency noise, a preamplifier was used with a gain of approximately 100 and a noise level of 1 or 2 nV/sqrt(Hz). The chip was directly dc coupled to the low-noise differential amplifier. A spectrum analyzer, which can measure the signal as low as 30 Hz, was used to characterize the noise performance. To ensure the best noise measurement, the multiplier was run from a battery to get a very clean supply for the noise test. Fig. 8 shows the measured performance. The low-frequency noise

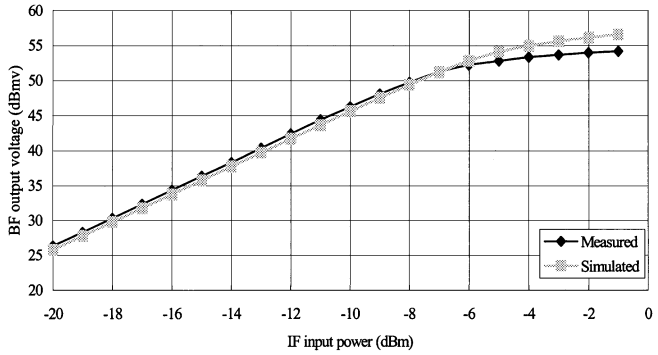


Fig. 6. Simulated and measured multiplier output voltage versus IF power at 11 GHz with BF of 10 MHz.

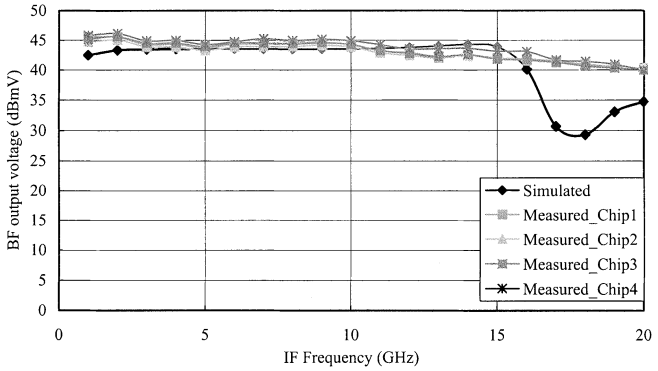


Fig. 7. Simulated and measured multiplier output voltage. The measured output voltage is 45 dBmV at the input power of −11 dBm, and the measured sensitivity was 1100 V/W. Output voltages of four chips on the same wafer were measured, demonstrating the consistent measured results.

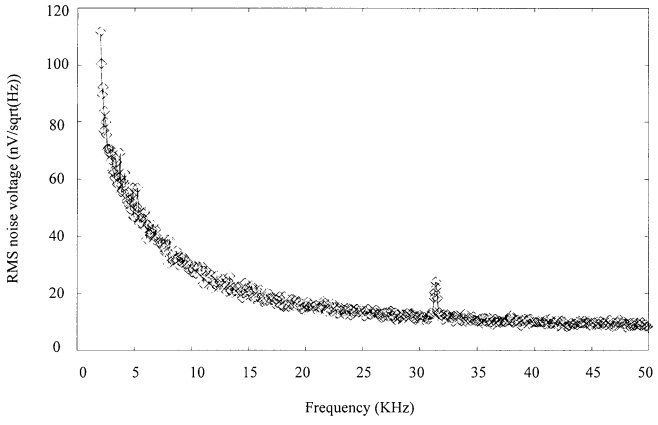


Fig. 8. Measured multiplier low-frequency noise from 1 to 50 kHz. The low-frequency noise and its corner frequency were estimated to be 10 nV/sqrt(Hz) and 15 kHz.

and corner frequency can be estimated to be 10 nV/sqrt(Hz) and 15 kHz. According to [12], the low-frequency noise of the InGaP–GaAs HBT multiplier is about half that of the InP HBT multiplier. This superior low-frequency noise performance is due to the few traps in energy levels of the InGaP–GaAs HBT, which compares very favorably with that of a conventional AlGaAs/GaAs HBT.

V. Conclusion

This paper has presented the development of a 1–17-GHz HBT analog multiplier and mixer that adopts a Gilbert cell multiplier. The highlight in this analog multiplier and mixer design is that input broad-band matching networks are used to broaden the bandwidth up to 17 GHz. It achieved a measured sensitivity of above 1100 V/W and a conversion gain of better than 9 dB from 1 to 17 GHz. The measured performance rivals that of the previously reported analog multipliers and mixers.

Acknowledgment

The authors would like to acknowledge the InGaP–GaAs HBT process support of the WIN Semiconductors Corporation, Taiwan, R.O.C. The authors would also like to thank Dr. W. Wilson, Australia Telescope National Facility, Marsfield, N.S.W., Australia, and P. Roberts, Australia Telescope National Facility, for noise measurement and Prof. C. K. Wang, National Taiwan University, Taipei, Taiwan, R.O.C., for his helpful discussion.

References

[1] K. Leong and R. G. Meyer, "Monolithic RF active mixer design," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 231–239, Mar. 1999.

[2] K. W. Kobayashi, R. M. Desrosiers, A. Gutierres-Aitken, J. C. Cowles, B. Tang, L. T. Tran, T. R. Block, A. K. Oki, and D. C. Streit, "A DC-20-GHz InP HBT balanced analog multiplier for high-data-rate direct-digital modulation and fiber-optic receiver applications," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 194–202, Feb. 2000.

[3] J. Wholey, I. Kipnis, and C. Snapp, "Silicon bipolar double balanced active mixer MMIC's for RF and microwave applications up to 6 GHz," in *IEEE Microwaves and Millimeter-Wave Monolithic Circuits Symp. Dig.*, Long Beach, CA, 1989, pp. 133–137.

[4] A. Y. Umeda, C. T. Matsuno, A. K. Oki, G. S. Dow, K. W. Kobayashi, D. K. Umemoto, and M. E. Kim, "A monolithic GaAs HBT upconverter," in *IEEE Microwaves and Millimeter-Wave Monolithic Circuits Symp. Dig.*, Dallas, TX, 1990, pp. 77–80.

[5] K. Osafune and Y. Yamauchi, "20-GHz 5-dB-gain analog multipliers with AlGaAs/GaAs HBTs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Boston, MA, 1991, pp. 1258–1288.

[6] L. M. Burns, J. F. Jensen, W. E. Stanchina, R. A. Metzger, and Y. K. Allen, "DC-to-Ku-band MMIC InP HBT double-balanced active mixer," in *IEEE Int. Solid-State Circuits Conf. Dig.*, San Francisco, CA, 1991, pp. 124–125.

[7] K. W. Kobayashi, L. T. Tran, S. Bui, A. K. Oki, D. C. Streit, and M. Rosen, "InAlAs/InGaAs HBT X-band double-balanced upconverter," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1238–1243, Oct. 1994.

[8] H. Wang, "A 1-V multi-gigahertz RF mixer core in 0.5-μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, San Francisco, CA, 1998, pp. 370–371.

[9] P. Weger, G. Schultes, L. Treitinger, E. Bertagnolli, and K. Ehinger, "Gilbert multiplier as an active mixer with conversion gain bandwidth of up to 17 GHz," *Electron. Lett.*, vol. 27, no. 7, pp. 570–571, Mar. 1998.

[10] J. Glenn, M. Case, D. Harame, B. Meyerson, and R. Poisson, "12-GHz Gilbert mixers using a manufacturable Si/Si–Ge epitaxial-base bipolar technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting Dig.*, Minneapolis, MN, 1998, pp. 186–189.

[11] Y. Imai, S. Kimura, Y. Umeda, and T. Enoki, "DC to 38-GHz distributed analog multiplier using InP HEMT's," *IEEE Microwave Guided Wave Lett.*, vol. 4, pp. 399–401, Dec. 1994.

[12] P. Roberts and W. Wilson, private communication.

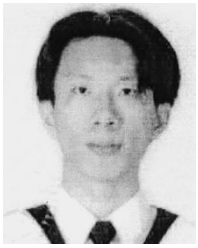
[13] K. W. Kobayashi, A. K. Oki, A. Gutierrez-Aitken, J. Cowle, L. T. Tran, T. R. Block, and D. C. Streit, "InP-based HBT technology for next-generation lightwave communications," *Microwave J.*, pp. 22–38, June 1998.

[14] *Using Series IV for Circuit Design E4602A + 24D*, Hewlett-Packard Company, Santa Rosa, CA, 1997.

[15] *Sonnet User's Manual*, Sonnet Software Inc., Liverpool, NY, 1998.

Bosen Tzeng received the M.S. degree in communication engineering from the National Taiwan University, Taipei, Taiwan, R.O.C., in 2001.

He then joined MedTek Inc., Hsin-Chu City, Taiwan, R.O.C., where he is currently involved with HBT power amplifiers and power control circuits for global system for mobile communication (GSM) handsets.



Chun-Hsien Lien received the B.E. degree in communication engineering from the National Chao-Tung University, Hsin-Chu City, Taiwan, R.O.C., in 1997, and is currently working toward the Ph.D. degree at the National Taiwan University, Taipei, Taiwan, R.O.C.

His main research interests are monolithic microwave/millimeter ICs.

Huei Wang (S'83–M'83–SM'95) was born in Tainan, Taiwan, R.O.C., on March 9, 1958. He received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Michigan State University, East Lansing, in 1984 and 1987, respectively.

During his graduate study, he was engaged in research on theoretical and numerical analysis of electromagnetic radiation and scattering problems. He was also involved in the development of microwave remote detecting/sensing systems. In 1987, he joined the Electronic Systems and Technology Division, TRW Inc. He was a Member of the Technical Staff and Staff Engineer responsible for MMIC modeling of computer-aided design (CAD) tools, MMIC testing evaluation, and design. He then became the Senior Section Manager of the Millimeter Wave Sensor Product Section, RF Product Center, TRW Inc. In 1993, he visited the Institute of Electronics, National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C., and taught MMIC-related topics. In 1994, he returned to TRW Inc. In February 1998, he joined the faculty of the Department of Electrical Engineering, National Taiwan University, where he is currently a Professor.

Dr. Wang is a member of Phi Kappa Phi and Tau Beta Pi.

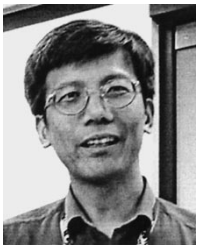
Yu-Chi Wang received the B.S. degree in physics from the National Central University, Taipei, Taiwan, R.O.C., in 1989, and the M.S. and Ph.D. degree in materials science and engineering from Rutgers University, New Brunswick, NJ, in 1994 and 1998, respectively. His doctoral dissertation concerned the design, molecular beam epitaxy (MBE) growth, fabrication, and characterization of $In_{0.5}(Al_xGa_{1-x})_{0.5}P$ power HEMTs.

In 1998, he joined Bell Laboratories, Lucent Technologies, Murray Hill, NJ, where he was a Member of Technical Staff, involved in the device design and process development of GaAs MOSFETs, 0.1-μm InAlAs/InGaAs HEMTs, and high-performance InP–InGaAs–InP double HBTs for 40-Gb/s lightwave circuits. He is currently the Director of the HBT Product Technology Development Division, WIN Semiconductors Corporation, Taiwan, R.O.C.

Pane-Chane Chao (S'80–M'82–SM'88) received the Ph.D. degree in electrical engineering from Cornell University, Ithaca, NY, in 1982.

He then joined the General Electric (GE) Aerospace Division, Syracuse NY. While with GE, he was responsible for GaAs MESFET and HEMT MMIC process technology development. He was the first to implement the low-resistance T-gate technology on GaAs HEMTs—setting an industry standard. Working with the University of Illinois in 1985, he and his team successfully demonstrated the world's first 60-GHz power pseudomorphic high electron-mobility transistor (pHEMT), opening the door for both military and commercial applications of this technology. In 1996, he joined Lockheed-Martin, Nashua NH, where he managed the Advanced HEMT MMIC Process Development Group to explore GaAs pHEMT, InP HEMT, metamorphic HEMT, and GaN HEMT technologies. In September 2000, he joined the WIN Semiconductors Corporation, Taiwan, R.O.C., where, as a Chief Technology Officer (CTO) and Senior Vice President, he leads the 6-in GaAs HBT and pHEMT technology development and manufacturing. In 2001, his team successfully demonstrated the first 6-in 0.15-μm pHEMT wafer in the world. He has authored and coauthored over 150 technical papers.

Dr. Chao is a Sanders Fellow. He currently serves as a Technical Program Committee member of International GaAs ManTech Conference.



Chung-Hsu Chen received the B.S. degree in physics from the National Taiwan Normal University, Taiwan, R.O.C., in 1954, and Ph.D. degree from the University of Minnesota at Minneapolis–St. Paul, in 1986.

He was a Principle Research Scientist with the Honeywell Corporation for three years, during which time he was involved with GaAs MESFET/HIGFET projects. He was with TRW Inc. for 11 years, during which time he was involved with GaAs power-amplifier testing, reliability, and layout. He is currently an Assistant Vice President with the Design Services Division, WIN Semiconductors Corporation, Taiwan, R.O.C. This division is responsible for GaAs pHEMT/HBT product engineering, reliability, and layout.